RESEARCH ARTICLE

Design of FPGA based NIOS-II Soft Core Processor for a wearable Tele Cardiac System

G. Kavya

Department of Electronics and Communication, S. A. Engineering College, Chennai, India.

ABSTRACT: Recently, the application fields of the embedded system have got expanded and the system complexity got increased. This has led to the need of high performance applications that use System on a programmable chip (SoPC). The integration of several hardware modules on a single chip is called SoPC, a single chip solution. This paper deals with the design of Nios II soft core processor using Qsys technology for a Telemedicine application. A soft-core processor is the central component of a system defined in software that can be synthesized in Programmable hardware called FPGAs. The design of SoPC for a Telecardiac system is done using Quartus II- Qsys system. Here the application of the system is validated on an Altera cyclone IV series FPGA chip. As the Qsys technology is used, the system provides high integration, high design flexibility, small volume and low power consumption. The system is configured by NIOS soft core CPU using Verilog HDL and C language. The proposed system can be used in Bio-Medicine (measuring various parameters using softcore) and control systems, etc. This paper discusses one such application in which continuous acquisition and analyzes of the acquired ECG signal is performed using a soft core Nios II processor implemented in Altera DE0 Nano FPGA board; and if any abnormality detected a SMS with calculated beat per minute and patient's location is sent to the caretaker or doctor through a GSM module. The major contribution in this work is that baseband operations of GSM module and GPS receiver are performed in separate soft processors and they are implemented in the same FPGA board.

KEYWORDS: FPGA, Tele cardiac System, GSM, GPS, Soft-core Processors

1. INTRODUCTION

Nowadays, FPGA technology is used in every application area for the replacement of discreet logic and implementation on system on a programmable chip (SoPC). With the SoPC system all the peripherals and glue logic in a bigger design area can be accommodated in a single FPGA. In general, the conventional hard-core processors are designed with a pre-plan on how to generate address decode and control signals. The major drawback in conventional type programming is that is that if errors occurred during validation, it is very difficult and complicated to make the necessary modifications. But the proposed methodology of using Nios II processor for the implementation eases this situation. System robustness and flexibility in developing the various modules are major advantages of single chip solution.The effectiveness of the proposed system is achieved by using FPGA cyclone board with the help of Quartus Altera II, Qsys, and Nios II EDS Eclipse. A Nios II hardware system is designed using Using the Quartus II software and Nios II Embedded Design Suite (EDS), can be used to create a software program that runs on the Nios II system and interfaces with components on the development boards.

ECG is a popular or widely used method to diagnose different types of arrhythmias and other disorders in the heart. The most important fiducial points in ECG signal are based on Wireless LAN and PDA; FPGA for QRS detection [1]; a web server and PIC Microcontroller for real time monitoring system of ECG signal [2] has been implemented in earlier literature. Other, implementation using FPGA includes particle swarm optimization P, Q, R, S, T, and U. Every point has a relation to electrical activity of the heart and it is vital for medical analysis.

The QRS complex formed during the ventricular contraction provides essential and fundamental information for ECG analysis due to its slope and magnitude. Now-a-days better solutions for filtering, removal of noise, feature extraction and enhancement are provided by high end processors and FPGA family. But, the systems that are existing today lack in multiprocessing capability. Hence the proposed system involves acquisition and real time analysis of the ECG signal using a FPGA board and a SMS is initiated and transmitted that has information about the heart rate and location of the patient to the patient's care taker and ambulance centre. The major tasks involved in the system implementation are filtering of ECG signal, QRS detection, Interpretation, GPS (Global Positioning System) acquisition and parallel tracking which are carried out by multiple Nios–II soft core processors implemented in ALTERA environment. Each core runs independently and coordinated with Avalon bus arbitration.

Pseudo noise generator using FPGA has been [3]; Public switched telephone Networks (PSTN) based and telemedicine system [4] based on Wireless Access Protocol (WAP); a physiological monitoring system [5] technique for placement problem [6] and improved Algorithm for Objects Distance Measurement in image Processing [3]. A portable system [7, 8] implemented using microcontroller that is capable of transmitting ECG signal to a remote PC for analysis was implemented. A

**Corresponding Author:* *drgkavya@saec.ac.in*

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smart diagnostic system [9] using FPGA that performs analysis on the criticality of a cardiac patient was analysed using FPGA. The major drawback of the above system is that the system did not have any wireless transceiver for communication purpose. Less than 60 minutes is known as "call to needle" time, within which the critical patient must be attended by the doctor in case of acute myocardial infarction [10].This has led to the development of a mobile Tele cardiac system [11] with GPRS transceiver and the functionality of the entire setup was verified in MATLAB environment and the same system was developed using ARM microcontroller. A lot of literature is found earlier that uses FPGA for the analysis of ECE signal. Few of them includes, ECG feature extraction [12] in real time; a robust QRS detection system [13] based; ECG monitoring device [14] that functions in Bluetooth frequency; design of Finite Impulse response filter for the removal of noise [8]; Implementation of wavelet fuzzy for Arrhythmia classification in ECG signal using wavelet fuzzy [15] was carried out. The advantage of the above system was that a remote central management unit receives the patient's bio signals but a drawback is that acquired signal is not processed at the patients end and no online analysis was performed. The above clearly reveals that there is no literature found that uses Nios –II softcore processor for parallel computation of patient biosignal.

2. MATERIALS AND METHODS

2.1 Existing Telemonitoring Technology

One of the major requirements in healthcare services includes a monitoring system that has the capability of bringing down the want of hospitalization. Monitoring systems that are commercially available is discussed in the following. The classification is also based on the research proposals done so far related to monitoring systems silver).

Online Recording and offline Analysis System

The systems under this category performs recording of the vital signals and real time classification or analysis is not performed. Holter monitor and Medtronic Reveal Insertable Loop recorder are few examples under this category. For example, a Holter monitor which is a portable device that continuously monitor the electrical activity of the heart for 24 hours or more is provided after the patient is discharged from the hospital. This helps the medical practioner to observe occasional cardiac arrhythmias. Medtronic Reveal Insertable Loop recorder is one that allows recording of ECG episodes for period's up to 14 months. These solutions have some advantages and some serious drawbacks. So, in the above systems, recording of ECG signal is done and offline analysis is performed on the signal.

Remote Real Time Monitoring Systems

In systems such as, Vitaphone (Daja 2001), QRS diagnostic, Cardio control and Active Corporation, the ECG signals acquired at the patient end are processed in a monitoring center placed remote. This clearly shows the limitation of the above systems i.e the analysis is not performed in the place where the signal is acquired. In Vitaphone a card is employed which is responsible for infrared transmission of the acquired ECG using to a mobile phone. Analysis of the ECG signal is performed in a service centre Some other systems like QRS diagnostic, Active Corporation, Cardio control, commercializes a product that permits visualization and recording. Later, the signals stored in PDA are received by a workstation for further analysis and printing of signals. So it is clear from this that analysis in patient side is restricted. Another drawback in this kind of system is that the normal ECG signal is also transmitted that forces in an inefficient use of wireless network. The worst condition occurs if there is non-availability of the network for a shorter moment which may lead to loss of the ECG signal and the risk occurs if the anomalies is found in the lost of ECG signal unless recorded or transmitted.

Local Real-Time Classification System

As the name implies, these systems make use of a local computers between sensors and the control centers or a hospital as a intermediary. These intermediary computers perform local real time monitoring by sending a alarm signal to the nearby hospital during inconsistent situation.

Home proposed by (Sachpazidis 2002), TeleMediCare and PhMon proposed by (Kunze 2002) are few examples of this system. In the above said systems, ambulatory sensors are fixed in patient through which the ECG is acquired and the same is transmitted in Bluetooth or DECT to a patient's local Personal Computer. This local PC installed with analyzing software activates an alert when the calculated parameters exceeds or reaches some threshold value defined by physician for a normal person. From the working of these systems it is clearly understood that the above systems reduces the moving area of the patient and sometimes it may restrict the patient with in a home. The other existing technology for telemonitoring is shown in Table1.

All the technology described in Table 1 are basically store and forward type or else the signal is transmitted to a data centre for further processing and no real time analysis is performed. Hence a Telecardiac system is proposed wherein continuous acquisition of ECG signal is performed and real time analysis at the patient end is done using FPGA. When the analyzer detects any abnormality, a SMS that contains the calculated heart rate along with the patient location is transmitted to the caretaker of the patient. But, the proposed system using softcore processors increases the mobility and the ability of a cardiac patient to regain his/her independence with free movement.

2.2 Proposed System

Controller required to implement any embedded solution are of three types and the choice of it depends on factors like cost, speed, space constraints, product life time, schedule of various events and flexibility of operation. One of the traditional approaches used by the designer is discrete off the shelf (OTS) processor from a multitude of vendors with wide range of features.

Table 1 Existing Telemonitoring Technology

Technology	***Description***
Toumaz Sensium	It performs continuous, wireless, intelligent monitoring at low-cost with the robustness and medical compliance.
Sensium	It consists of wearable sensor nodes connected to a base station which in turn is linked to target stations.
Lifelink	This employs a mobile for real-time telemonitoring associated with a diagnostic facility to command and control remote medical devices.
Corventis	Data is collected by a body worn device that transmits the same data through zLink - to a hosted application for further analysis and storage a small portable device (similar to a cell phone).
CardioNet	Ambulatory cardiac monitoring service
MedNet	Data transmitted from the patient's heart monitor to Bluetooth enabled cell phones.
CardioMessenger II	This technology use medical implants for acquiring the signal. The exterior device receives the data sent by the implant and forwards the information via the cellular phone network to the service center

These microprocessors are implemented as an ASIC with specific peripheral set under this category uses a Personal Digital Assistant (PDA).But selecting an OTS processor to meet the application cost and requirement is a time consuming process. Sometimes these processors may not meet the specified requirements. In that case these processors have to be tailored with some other custom logic.

The second type involves a portion of dedicated silicon on an FPGA, and they are termed as hard processor core. The designers using these types of processors suffer from inability to adjust the core for the required application and there is no flexibility to add or remove additional processors. The third type known as soft core Processors, proposed in our design for telecardiac system is the one that uses entirely the logic primitives of FPGA. Soft core processor is a best choice because of the amount of flexibility because of its configurable nature. There is no longer usage of specific set of peripherals because soft core processors enable the designer to add or remove peripherals from the SoPC (System on Programmable chip) based on the system requirement. The proposed system gets the benefit of using multiple soft core processors and executing the tasks in parallel.

The main blocks of any telemetry system are data acquisition, processing module and a communication network. Hence the proposed tele cardiac system as shown in Fig.1 includes three soft processor cores for performing the above operations. Core 1 for ECG signal analysis, interpretation and for decision making; Core 2 performs GSM baseband operations like channel encoder, Interleaver and GMSK modulator; Core 3 have been implemented to perform operations of GPS receiver like signal acquisition, tracking and for synchronization of data received from the RF front end.

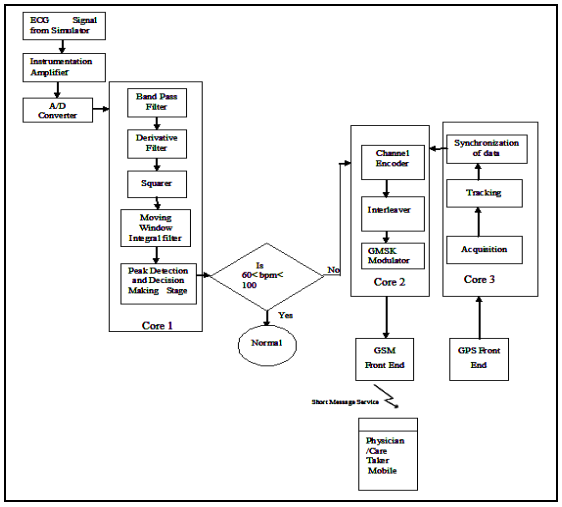
3. RESULTS AND DISCUSSION

Processor core implemented in FPGA with custom hardware is referred as System on programmable chip (SoPC).Nios II, a 32 bit embedded processor have been specifically designed for the Altera FPGA family. FPGA implementation of the proposed system hardware is shown in Figure 1.

The various blocks pertaining to Arrhythmia detector, GSM baseband processor and GPS data processing modules as discussed in previous sections are implemented in Altera DE0 Nano FPGA board that contains Altera Cyclone IV EP4CE22F17C6N FPGA device; Altera serial configuration device EPCS64; onboard USB blaster for programming; 32 Mbytes of SDRAM; 4Mbytes of flash Memory and RS-232 Transceiver.

Altera USB Blaster Driver software is used for the communication between the host computer and the FPGA Nano board. An interface between the host computer and the device is provided by Philips ISP1362 USB controller.E^2PROM chip on DE0 board is used to store the Configuration data for the cyclone–IV FPGA.As the power supply is switched on, automatically the configuration data gets loaded into FPGA from the memory cell i.e E^2PROM. JTAG programming (Joint Test Action Group) and Active Serial Programming (AS) are the two ways by which user programming can be downloaded into FPGA. Out of the two methods available, JTAG programming has a disadvantage that configuration will be lost in the situation of power off. But its counterpart, (i.e) in AS programming, power on/off is not a issue and the data is made available during the situation of power off also. Loading of data into Cyclone IV FPGA is done by the on board configuration device

EPCS64. This makes as programming as a best choice in programming the FPGA.



The inbuilt SoPC builder option in Quartus is used to build the processor core along with set of peripherals like timers, on chip/off chip memory elements and bus architecture interconnected with Avalon Bus Protocol for interface purposes. The proposed system is implemented with three processor cores: cpu_0 for ECG analysis; cpu_1 for GSM Baseband processes and cpu_2 for GPS data processing application.

The proposed system targeted on Cyclone series FPGA has been implemented in the Altera's Quartus software environment.In the on–chip memory (Configurable ROM) of FPGA, details such as phone number and the analyzed values on the ECG signal is stored. Beats per minute (bpm) for a normal person ranges between 60 and 100. Hence, an ATTENTION command is initiated to SIM 900A through UART if the decision making circuit assesses a worst situation when bpm is not in the normal range.

The arrhythmia detector designed using softcore processor is connected to a compact Dual band GSM/GPRS SIM 900A module that has the capability of delivering signals such as voice, data and fax. Access to GSM network is provided by a valid SIM card that is present inside a SIM card holder that is of plug in type. LM7805, a voltage regulator is used to provide +4.1 V power supply to the GSM modem. The status of the GSM module like power on, Network access and registration, GPRS connectivity etc is shown by LED display. For example, establishment of GSM connectivity is shown by blinking of LED in step of 3 second assuming that the power supply to the board and valid SIM card is available. Figure.3. Shows the alerting SMS received in the mobile phone along with abnormal heart beat rate and the location of the patient.

4. CONCLUSION

The proposed work has been validated using an ECG simulator and Altera DE0 Nano FPGA board. Major work in this paper is the design of baseband operations of GSM module and GPS receiver in separate soft processors and they are implemented in the same FPGA board along with the ECG analyser module. Real time acquisition of ECG signal integrated with the proposed system could be carried out as a future work.

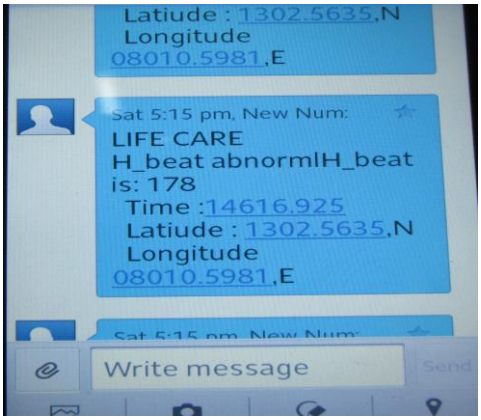


Figure 3 Heart beat per minute with location received in a Mobile Phone

REFERENCES

[1]. Li Nian qiang., Hou Si-Yu., cui Shi-Yao ., 2010. Application of Distributed FIR Filter based on FPGA in the analyzing of ECG signal. International Conference on Intelligent System Design and Engineering Application (ISDEA), 335-338.

[2]. Lin, Yusan Hsiang., 2004. A Wireless PDA based Physiological monitoring system for patient Transport. IEEE Transactions on Information Technology in Biomedicine, 8, 39-47.

[3]. Daniel Lucani., Giancarlos Cataldo., Guillermo Villegas., 2006. A portable ECG monitoring device with Bluetooth and Holter capabilities for Telemedicine application. EMBS Annual International Conference, IEEE, 5244-5247.

[4]. Ghulam M. Bhat., Muhammad Mustafa., Shabir A. Parah., Javaid Ahmad., 2010. Field Programmable gate array (FPGA) implementation of novel complex PN- code generator-based data scrambler and descrambler. Maejo Int.J.Sci.Technol, 4, 125-135.

[5]. Hung., Kevin., 2003. Implementation of a WAP based telemedicine System for Patient monitoring. IEEE Transactions on Information Technology in Biomedicine, 7, 101-107

[6]. Akbarpour,H., Karimi,G., Sadeghzadeh,A, 2015. Discrete Multi Objective Particle Swarm Optimization Algorithm for FPGA Placement, International Journal of Engineering transcations C: Aspects, 28(3) 410-418.

[7]. Mohammad Saleh Nambakhsh., Vahid Tavakod.i., 2008. FPGA –Core Defibrillator using wavelet –

Fuzzy ECG arrhythmia classification. Conf. Proc. IEEE Eng Med Biol Soc. , 4828-4831.

[8]. Rajendran,V.G., Jayalalitha,S., Anushaa,R Karpagalakshmi, S., Karthikeyan,S 2016. GSM based physiological monitoring of patient by using zigbee. Far East Journal of Electronics and Communications, Special Volume, Part I, 33 – 41.

[9]. Stojvanic, R., Karadaglic,D., Mirkovic,M., Milosevic.D, 2011. A FPGA system for QRS Detection based on Integer Wavelet Transform. Measurement Science Review, 11,131-138.

[10]. Saurabh Prakash., Venkatesh,V 2013.Real time monitoring of ECG signal using PIC and web server. International Journal of Engineering and Technology (IJET), 5, 1047- 1053.

[11]. Voskarides,S.Ch., Pattichis,C.S., Istepanain,R, 2003.Practical evaluation of GPRS use in Telemedicine System in Cyprus. Proc. Inf.Tech Applns. In Biomedicine,4th Conf., U.K , 39-42.

[12]. Mitra,S., Bera, J., Mitra,M., Sengupta, S, 2006 Wireless Communication based Portable Telecardiology system for rural health care. IETE Technical Review, 23,277-282.

[13]. Roy Chowdhury,S., Saha,H, 2006. Development of an FPGA based smart embedded system for Rural Telediagnostic Applications. IETE Technical Review, 23, 297-304.

[14]. T.David A Sandler., 1999. Call to Needle Times after Acute Myocardial Infarction. BMJ, 318, 597-598.

[15]. Thulasi Bai,V., Srivatsa,S.K, 2008. Design and implementation of mobile Telecardiac system. J SCI IND RES, 67, 1059-1063.

[16]. Asish Shukla., Luca Macciarrulo ., 2008. A fast and accurate FPGA based QRS detection system Engineering in Medicine and Biology Society.30th Annual International Conference of the IEEE, 4828-4831.

[17]. Weichu Hu.,Chun Cheng Lin., Liang Yu Shyu., 2011.An Implementation of a Real time and Parallel processing ECG feature extraction algorithm in a field programmable Gate array. Computing in Cardiology, 801-804.

[18]. G Kavya., V Thulasibai. VLSI implementation of telemonitoring system for high risk cardiac patients. Indian Journal of Science and Technology 7 (5), 571.

[19]. Kavya,G., ThulasiBai,V, Implementation of GPS Signal Acquisition and Tracking in FPGA. IJRET: International Journal of Research in Engineering and Technology.

[20]. Kavya,G., ThulasiBai, V, 2014. Wearable advanced single chip ECG telemonitoring system using SoPC. IEICE Electronics Express 11 (6), 20140097-20140097.

[21]. Kavya,G., Bai, VT, VLSI Technology for Real Time Monitoring System of High Risk Cardiac Patients. Studies on Ethno-Medicine 8 (3), 305-315.

[22]. Kavya,G., VT Bai, VT, A Literature Survey on Telecardiac Systems and Arrhythmia Classification. Digital Signal Processing 4 (3), 86-91.

[23]. Zivarian,H., Soleimani,M., DoostMohammadi, MH, 2017. Field Programmable Gate Array–based Implementation of an Improved Algorithm for Objects Distance Measurement. International Journal of Engineering (IJE), Transactions A: Basics, 30(1) 57-65.